TMSST2
LGA771, LGA775, and PGA604 Socket Hardware Support Instruction Manual

(Includes TMSDPH2 SOCKET T/J 771/775 LGA

Installation instructions)

www.tektronix.com
071-1665-02

Tektronix

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of a larger system. Read the safety sections of the other component manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

D Head.

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

The inputs are not rated for connection to mains or Category II, III, or IV circuits.

Power Disconnect. The power cord disconnects the product from the power source. Do not block the power cord; it must remain accessible to the user at all times.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate in Wet/Damp Conditions.

Do Note Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Terms in this Manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Symbols and Terms on the Product

- DANGER indicates an injury hazard immediately accessible as you read the marking.
- WARNING indicates an injury hazard not immediately accessible as you read the marking.
- CAUTION indicates a hazard to property including the product.

The following symbol(s) may appear on the product:

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Environmental Considerations

This section provides information about the environmental impact of the product.

Product End-of-Life Handling

Observe the following guidelines when recycling an instrument or component:

Equipment Recycling. Production of this equipment required the extraction and use of natural resources. The equipment may contain substances that could be harmful to the environment or human health if improperly handled at the product's end of life. In order to avoid release of such substances into the environment and to reduce the use of natural resources, we encourage you to recycle this product in an appropriate system that will ensure that most of the materials are reused or recycled appropriately.

The symbol shown to the left indicates that this product complies with the European Union's requirements according to Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). For information about recycling options, check the Support/Service section of the Tektronix Web site (www.tektronix.com).

Restriction of Hazardous Substances

This product has been classified as Monitoring and Control equipment, and is outside the scope of the 2002/95/EC RoHS Directive. This product is known to contain lead, cadmium, mercury, and hexavalent chromium.

Preface

This document contains specific information about the TMSST2 LGA771, 775, and PGA604 Socket Hardware support product and contains information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating a microprocessor support product with the logic analyzer, you need only this manual to set up and run the probe adapter (processor unit and probe head).

Conventions Used in this Manual

The following icon is used throughout this manual:

Sequence Step

Manual Terms

The manual uses the following terms:

- **GTLREF** (Gunning Transceiver Logic Reference)
  The GTL+ inputs require a reference voltage (GTLREF) which is used by the receivers to determine if a signal is a logical 0 or 1.
- **Land**
  Land is an alternate name for a pin and is associated with LGA (land grid array) socket pads on a circuit board.
- **Reference voltage**
  The voltage threshold on the input receivers of the preprocessor unit.
- **Termination voltage**
  The voltage to which the receive signals are terminated.

Getting Started

The probe adapter (preprocessor unit and probe head) is an interposer design that allows the logic analyzer to acquire data from a microprocessor in the operating environment with little effect on the DUT.

To accomplish this, the probe adapter is connected to the DUT, and then the microprocessor is connected to the probe head. Signals from the microprocessor-based system flow through the probe cables to the logic analyzer.

The TMSST2 product includes:

- CD-ROM with PUB32G11 software and manual
- TMSST2 preprocessor unit

***NOTE**. To acquire signals from the DUT, you need compatible cables, probes, and probe head to complete the connection between the logic analyzer and the DUT. Contact your Tektronix sales representative for information about these other products.*

For optional and standard accessories for this product, see *Accessories* on page 16.

For a list of replaceable parts, see page 13.

Logic Analyzer Configuration

To use the preprocessor unit and probe head to acquire most signals, you need a Tektronix logic analyzer with four merged TLA7AX4, 450 MHz, logic analyzer modules.

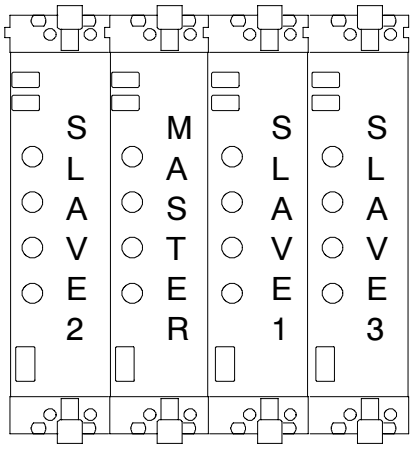
All signals are acquired through a combination of P6860 probes and TMSCAB1 cables connected to the logic analyzer. The P6860 probes should already be labeled; if you need to apply labels, refer to the instructions that came with your probe documentation.

Refer to the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction manual*, Tektronix part number 071-1059-xx, for more information about the P6860. Access the latest version of the manual from the Tektronix.com Web site.

Master and Slave Module Configuration

The modules must be configured and merged as shown.

- The memory depth is automatically based on the shallowest memory depth of the modules.
- The term *Master module* refers to the second module of a 4-wide module configuration. The term Slave module refers to the modules to the left or right of the Master module.



Connect the P6860 Probes and TMSCAB1 Cables

CAUTION. *To prevent damage to the probe and preprocessor unit, always position the probes perpendicular to the footprint on the circuit board. Incorrect handling of the probe while connecting to or disconnecting from the preprocessor unit can damage the probe.*

Use two P6860 probes and five TMSCAB1 cables to connect the TLA7AX4 logic analyzer modules to the preprocessor unit. If you need to attach labels to TMSCAB1 cables, refer to page 17.

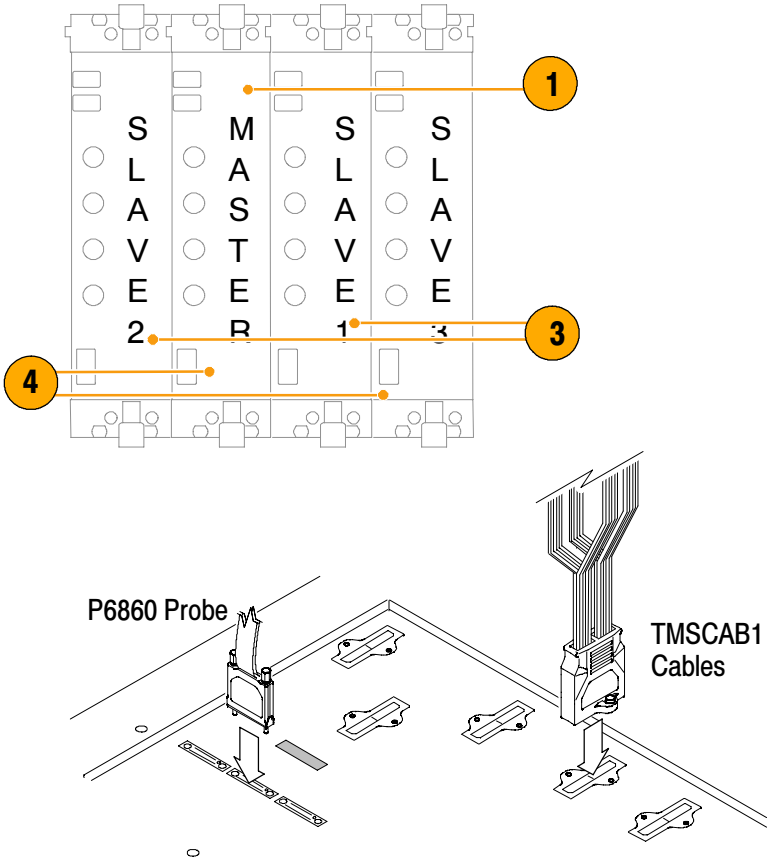
TMSCAB1 Cables

1. From the Master module, match the label on the TMSCAB1 cable with the corresponding connector label on the preprocessor unit and connect the cable. The TMSCAB1 cable connector is keyed for correct alignment to the preprocessor unit.
2. Use care to evenly tighten both screws on the module end of the probes or cables until they are snug. First slightly tighten both screws, then snug each screw to 4 in-lbs (max).
3. Repeat step 1 to attach the TMSCAB1 cables to the Slave1 and Slave2 modules.

P6860 Probes

4. Match the A, D, C, and E probes from the Slave3 and Master module with the corresponding D3/D2 and A3/A2, D1/D0 and A1/A0, C1/C0 and C3/C2, and E3/E2 and E1/E0 connector labels on the preprocessor unit. The P6860 probe connector is keyed for correct alignment to the preprocessor unit.

Quick Tip. To prevent faulty connections and loss of data, check that the probe board connections are clean and free of debris.



Configure the Preprocessor Unit

To acquire the necessary signals from the DUT, the preprocessor unit generates two tracking voltages referred to as V_{TERM} and V_{REF}. V_{TERM} is the voltage to which most of the received target signals are terminated, while V_{REF} is the reference to which the attenuated target signals are compared.

You can configure the preprocessor unit to use one or more of the GTLREF signals and combine these signals with an offset voltage using the jumpers on top of the preprocessor unit. (See Figure 1.)

Review the schematic diagram in Figure 1 to understand how the jumpers and offset adjustments define the reference and termination signals. The connectors provide access for monitoring the voltages.

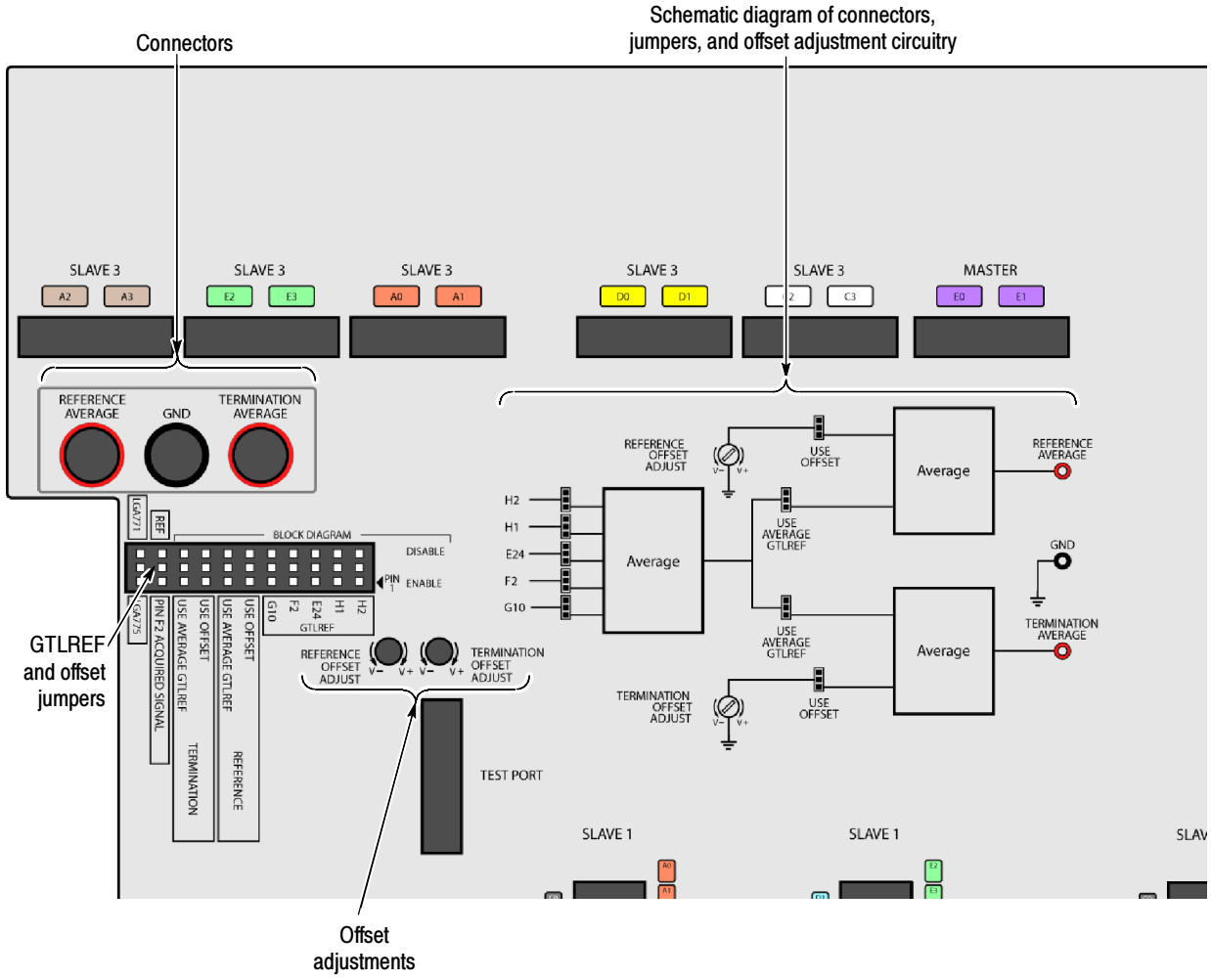


Figure 1: Preprocessor jumper, adjustment, and connector locations

Select a GTLREF Signal

The most common and straightforward scenario is to select an individual GTLREF signal using the jumpers to generate a reference and termination voltage. When you enable a GTLREF signal, the average voltage is equal to the GTLREF voltage.

As an alternative to a single GTLREF selection, you can combine two or more GTLREF signals that result in the average of all the contributors. The next step beyond a GTLREF only selection is to add a DC offset. The resultant voltage continues to track GTLREF. Refer to the following combined calculation:

V_{REF} or V_{TERM} = ((V_{OFFSET} - V_{GTLREF_AVG}) x 0.130) + V_{GTLREF_AVG}

If you choose only the offset voltage to define the termination or reference voltage, a weighting factor is not used and the full magnitude offset voltage defines the resultant voltage.

For example, you selected a GTLREF signal that equals 0.7 V, the AVERAGE GTLREF jumper is enabled, and you are using an offset voltage to provide +0.05 V of offset. The resultant voltage would be 0.75 V.

To set this offset voltage, adjust to:

V_{OFFSET} = 7.69 (V_{RESULT} -V_{GTLREF_AVG}) + V_{GTLREF_AVG}
= 7.69 (0.75-0.70) + 0.70
= 1.0845 V

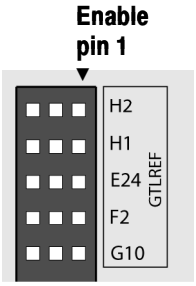
To summarize, the offset voltage source must be at 1.08 V to provide the +0.05 V of offset (in combination with an averaged GTLREF signal equal to 0.7 V). Therefore, if the AVERAGE GTLREF jumper is moved to the disabled position, an offset only selection sets the resultant voltage at 1.08 V.

***NOTE**. All jumpers and connectors are located on top of the preprocessor unit.*

Average a GTLREF Signal

To average GTLREF signals, enable one or more of the GTLREF jumpers. (See Table 1.)

Table 1: GTLREF Enable jumpers

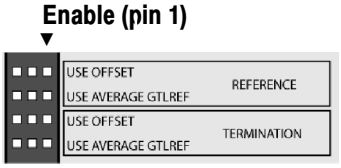
Jumpers	LGA771 and 775 Microprocessor pin name	PGA604 Microprocessor pin name	Default pin position
	H2	F23	2-3 Disable
	H1	F9	1-2 Enable
	E24	W23	2-3 Disable
	F2	AD30	2-3 Disable
	G10	W9	2-3 Disable

Combine Averaged GTLREF Signals with Offset Voltages

Use the four sets of jumpers shown in Table 2 to combine the averaged GTLREF signal with a separate independent fixed offset voltage.

- Enable both sets of REFERENCE jumpers to generate a combined reference voltage.
- Enable both sets of TERMINATION jumpers to generate a combined termination voltage.

Table 2: Reference and termination jumpers

Jumpers	Jumper name	Default pin position
	REFERENCE	
	USE OFFSET	2-3 Disable
	USE AVERAGE GTLREF	1-2 Enable
	TERMINATION	
	USE OFFSET	2-3 Disable
	USE AVERAGE GTLREF	1-2 Enable

When you enable both the AVERAGE GTLREF and the OFFSET jumpers, the resultant termination and reference voltages are weighted (20 to 3) to provide a substantial degree of GTLREF tracking.

Even when the AVERAGE GTLREF jumper is disabled for both the reference and termination voltage, the average GTLREF signal is used to generate a reference voltage for 13 target signals. To guarantee that the average GTLREF signal is at an appropriate level, the average GTLREF signal defaults to the processor land H1 on the DUT, if all five jumpers are placed in the disabled position.

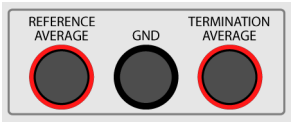
NOTE. *If the land H1 on the DUT is the desired GTLREF signal, use the jumper on the preprocessor unit to enable it rather than relying on defaults. The land H1 default is only intended to prevent undefined conditions from occurring.*

Adjust GTLREF Offset Voltage

To use either reference or termination offset voltage, you must enable it. (See Table 2 on page 5.) Connect a voltmeter to the Reference or Terminator connector and GND on the preprocessor unit using standard cables. The voltage is the averaged signal that is used by the front-end comparators (reference average and termination average). If the manual USE OFFSET jumper is the only jumper enabled, the voltage at the connector directly reflects the manual offset voltage.

CAUTION. *Connecting a voltage source to the Reference or Terminator connectors can damage the preprocessor unit. Only use standard cables to read the manual offset voltage.* (See Table 3.)

Table 3: Reference and terminator connectors

Connectors	Name
	TERMINATION AVERAGE
	GND - MEASUREMENT REFERENCE
	REFERENCE AVERAGE

Adjust the offset voltage with a small screwdriver, if necessary. (See Table 4.) Turn the potentiometer clockwise to increase the voltage. The range of the offset voltage is from 0.4 V to 1.0 V.

Table 4: Offset voltage adjustments

Adjustment	Name
	TERMINATION OFFSET ADJUST
	REFERENCE OFFSET ADJUST

NOTE. *To resolve acquisition errors, adjust the reference voltage. To resolve target-system loading issues, adjust the termination voltage.*

LGA771/LGA775 jumper. Select the socket that your target processor uses.

Table 5: LGA771/LGA775 jumper

Socket name	Pin position
PGA604	1-2 (default)
LGA775	1-2 (default)
LGA771	2-3

F2 ACQUIRED SIGNAL jumper. Enable REF if the signal is a GTLREF signal, otherwise ACQUIRED SIGNAL is the default.

Table 6: F2 Acquired signal jumper (AD30 for PGA604)

Jumper name	Pin position
Acquired signal	1-2 (default)
REF	2-3

XTGIP and Test Ports. Not used.

Connect the Probe Head to the DUT

CAUTION. *To prevent static damage to the microprocessor, preprocessor unit, probe head, probes, and module, handle components only in a static-free environment. Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor and probe adapter.*

WARNING. *To prevent personal injury or damage to the preprocessor unit, do not open the preprocessor unit. There are no operator-serviceable parts inside the preprocessor unit. Refer servicing of internal parts in the preprocessor unit to Tektronix authorized personnel only. External parts may be replaced by qualified service personnel.*

Airflow Clearance

Table 15 lists airflow clearances on all sides of the preprocessor unit that are needed when using the probe head.

Table 7: Preprocessor airflow clearance

Side of the unit	Required clearance
Required airflow clearances for the preprocessor	
Front, top, left side	5.08 cm (2 in)
Back	7.60 cm (3 in)
Bottom, right side	0.635 cm (0.250 in)

Tools

- **Required.** Use a flatbladed screwdriver (0.1 inch tip width) to tighten the probe head to the DUT.
- **Optional.** A torque wrench helps to ensure reliable connections by meeting the nominal torque values. Unless noted otherwise, tighten screws to 8 in-lbs.

CAUTION. *To prevent damage to the LGA771 and 775 sockets, minimize the amount of times the processor is inserted into the probe head. The probe head is designed to withstand 20 processor insertions. Once the LGA771 or 775 sockets are damaged, the probe head cannot be repaired. If great care is taken during processor insertion, the cycle life of the probe may be extended.*

Use the following steps to install parts:

Probe Head Installation

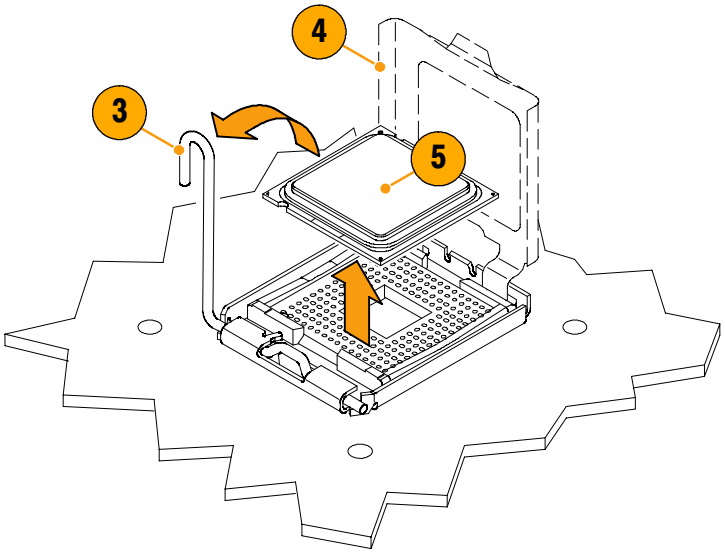
CAUTION. *To prevent damage to the socket, do not touch the springs in the socket.*

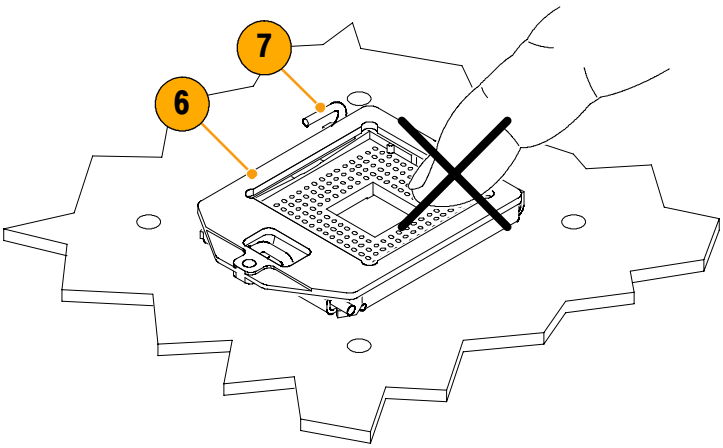
NOTE. *To connect the TMSSPH1 probe head, see the TMSSPH1 PGA604 Socket F Probe Head Support Instructions Manual (071-2001-XX).*

Use the following steps to connect the TMSDPH2 probe head to the DUT.

1. Power off the DUT. It is not necessary to power off the logic analyzer.
2. Power off any probe heads (or preprocessor unit) that may be attached to the DUT.
3. Open the load lever.
4. Open and remove the load plate.
5. Remove the microprocessor from the DUT.
6. Attach the custom load plate.

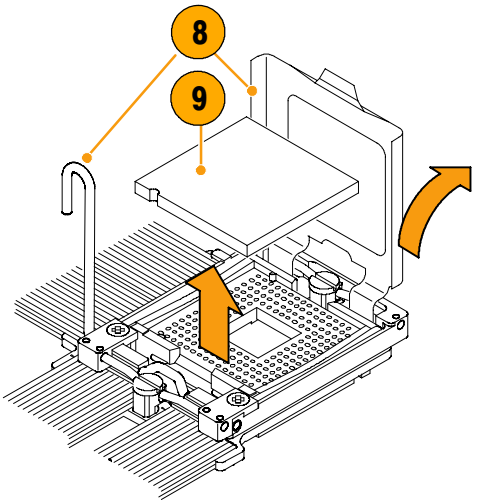
   Load plates are vendor-specific. Use the load plates marked with an “F” with the Foxconn socket and the load plate marked with a “T” with the Tyco socket.
7. Close the ZIF lever.





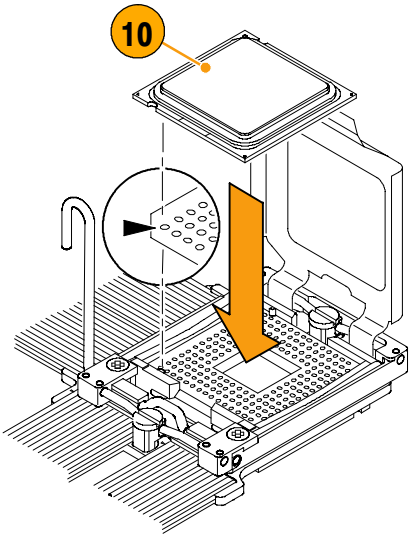
Use the following steps to connect the microprocessor to the probe head socket and DUT:

CAUTION. *To prevent damage to the springs in the processor socket or damage to the preprocessor unit caused by power and ground shorts, check that the pin 1 indicator on the probe head aligns with the pin 1 indicator on the DUT. (See the additional Caution on page 8.)*

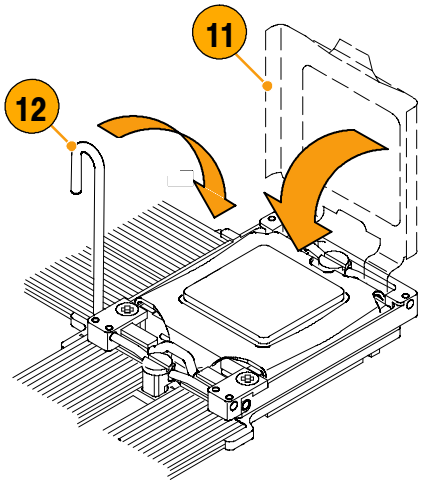


8. Open the ZIF lever and load plate on the probe head.

9. Remove the socket cover.



10. Install the microprocessor, carefully aligning pin 1 indicators (▶).



11. Close the probe-head load plate.

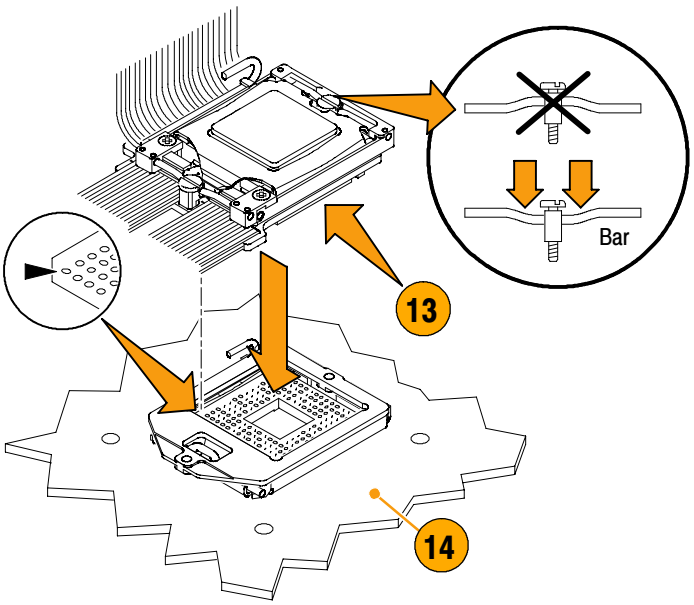
12. Close the ZIF lever.

Check the following items on the probe head:

- The bar is positioned as shown
- You have correctly located pin 1

13. Do not remove the socket adapter from the bottom of the probe head.

14. Attach the probe head to the DUT carefully aligning pin 1 indicators (▶).



15. Tighten the two screws to the custom load plate as shown.

To install the LGA771 heat sink hardware, see page 11.

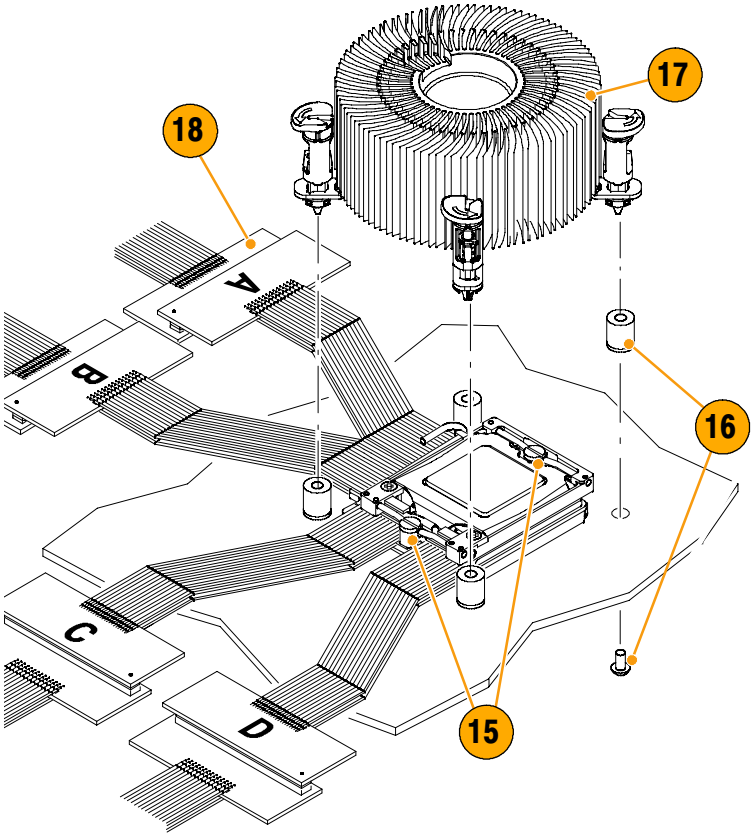
LGA775 heat sink hardware kit. Follow these steps to attach the probe head and the LGA775 heat-sink kit hardware:

16. Thread the standoffs onto the screws as shown.

17. Snap the heat sink into the standoffs(4).

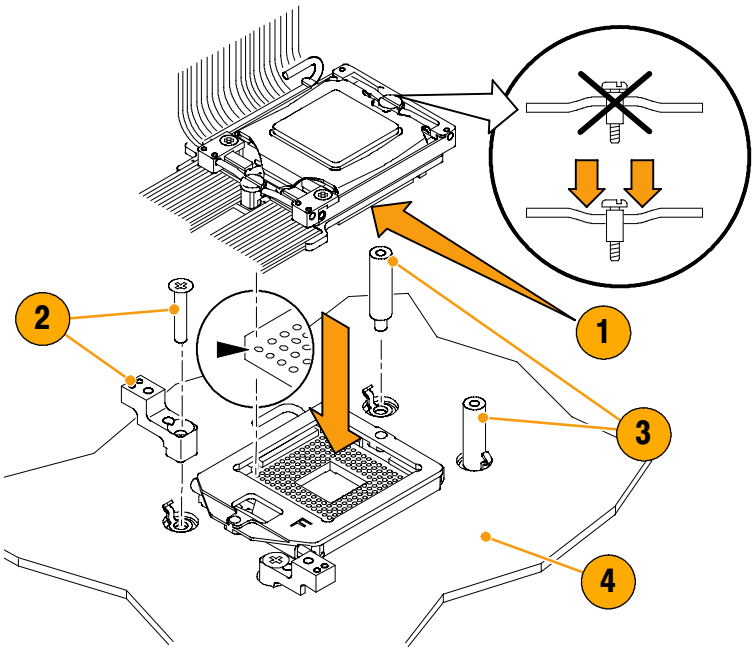
18. Connect the probe head cables to the preprocessor unit cables (snap into place) paying close attention that the labels on the paddle boards match: A to A, and so forth.

19. Apply forced-air cooling across the microprocessor and heat sink to keep the microprocessor from overheating unless you are using a forced air-cooled heat sink and fan assembly.

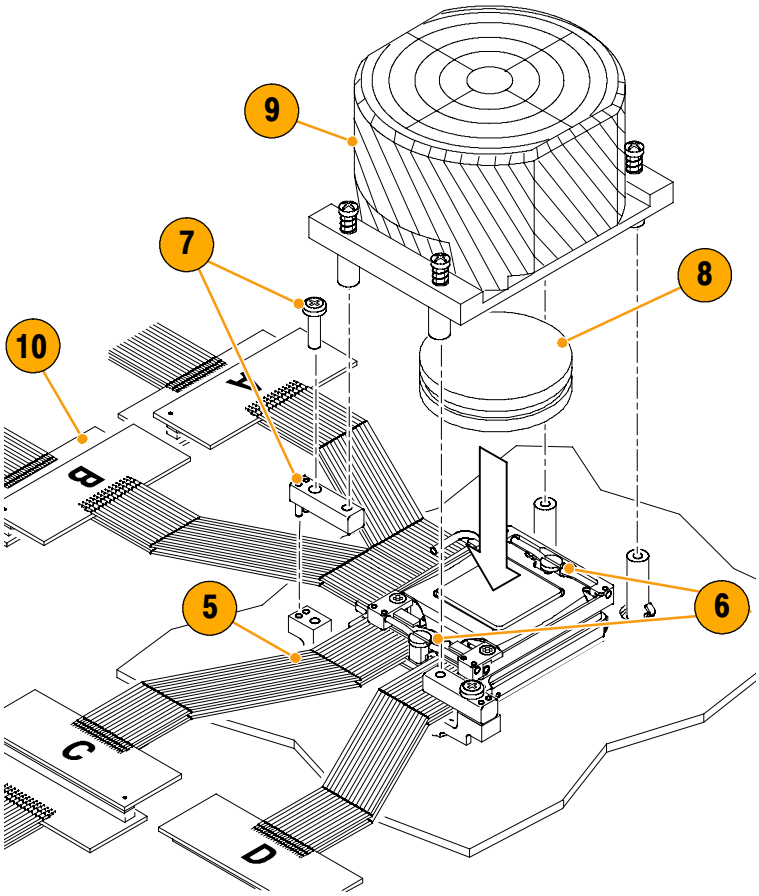


LGA771 heat sink. follow these steps to attach the TMSDPH2 probe head and the LGA771 heat sink kit hardware:

1. Do not remove the socket adapter from the bottom of the probe.
2. Using the flat head screws, attach two heat sink bottom brackets to the DUT.
3. Attach two standoffs to the DUT.
4. Attach the probe head to the DUT, aligning pin 1 indicators (▶).



5. Dress the cables over the bottom heat sink bracket.
6. Tighten the two screws to the custom load plate as shown.
7. Using the pan head screws, attach two heat sink top brackets as shown.
8. Apply thermal grease to the top of the copper spacer.
9. Install the heat sink.
10. Connect the probe head cables to the preprocessor unit cables (snap into place) paying close attention that the labels on the paddle boards match: A to A, and so forth.
11. Apply forced-air cooling across the microprocessor and heat sink to keep the microprocessor from overheating unless you are using a forced air-cooled heat sink and fan assembly.

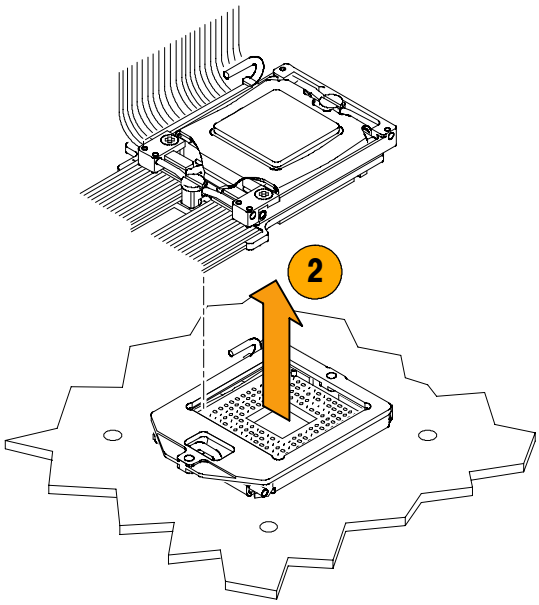


Probe Head Removal

Follow these steps to remove the probe head from the DUT:

CAUTION. *To prevent damage to the springs in the probe-head socket, always insert the socket cover when the probe head is not in use. (See Step 9 on page 9.)*

1. Power off the DUT and preprocessor unit. The power switch for the preprocessor unit is located on the back of the preprocessor unit. It is not necessary to power off the logic analyzer.
2. Reverse the steps in the previous illustrations to remove the probe head.
3. Store the probe head.

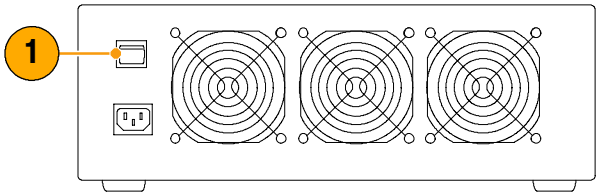


Applying and Removing Power

To apply power to the preprocessor unit and DUT, follow these steps:

1. Make sure the power switch on the preprocessor unit is in the off position.
2. Plug the AC power cord into the IEC connector on the back of the preprocessor unit.
3. Plug the AC power cord into an electrical outlet.
4. Power on the preprocessor unit using the switch at the back of the preprocessor unit. A green, power-on LED lights on the front of the preprocessor unit, indicating that the preprocessor unit is active.
5. Power on the DUT.

   To remove power from the DUT and the preprocessor unit, reverse the preceding steps.



Replaceable Parts List

Refer to the following table to view and reorder replaceable parts for the preprocessor and probe head.

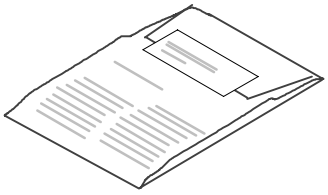
Page number	Step	Quantity	Description	Part number[1]
8	4	1	Load plate, bottom, for FOXCONN socket	386-7398-XX
8	4	1	Load plate, bottom, for Tyco socket	386-7400-XX
9	9	1	Socket cover	200-4843-XX
10	13	1	Socket adapter; SMD, BGA to LGA, pin header, 769 POS	131-7494-XX
2	1	1	Cable assembly (for preprocessor unit) with labels	012-1661-51

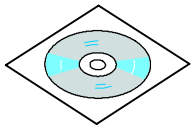
1 **To order replaceable parts for the heat sink kits or other probe heads, refer to the instructions that came with that product.**

***NOTE**. For a list of standard and optional accessories (including heat sink kits), refer to page 16 .*

Installing the Software

***NOTE.** Before you install any software, verify that the microprocessor support software is compatible with the logic analyzer software by comparing the version number on the CD to the Tektronix logic analyzer system software.*





To install the TMSST2 software on the Tektronix logic analyzer, follow these steps:

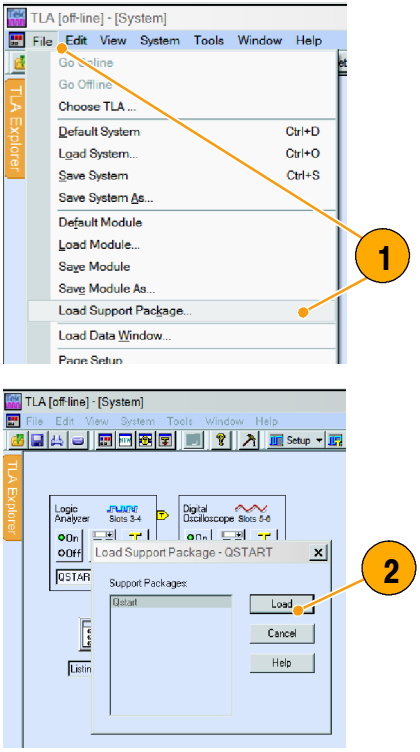
1. Insert the CD in the CD drive.
2. Select the Windows Start button > Control Panel > Add/Remove Programs.
3. Select the Add New Programs button on the left side of the display.
4. Select the CD or Floppy button.
5. Follow the on-screen instructions to install the software.

To remove or uninstall software, use the Add or Remove Programs utility in the Windows Control Panel. Close all windows before you uninstall any software.

Support Package Setup

After installing the software, you need to load the PUB32G11 setup file. Follow these steps:

1. Open a system window and from the file menu, select Load Support Package.
2. In the Load Support Package dialog box, select the support and click load.
3. Follow the on-screen instructions.



Reference

Circuit Description

The preprocessor unit and probe head processes all signals on the microprocessor before the logic analyzer captures the signals. The TMSST2 product performs the following functions:

- Latches signals within a narrow valid window
- Demultiplexes quad-pumped, source-synchronous signals
- Deterministically synchronizes source-synchronous data signals to BCLK

Latched Operation

The signals are processed according to their type. Following is a description of each type:

4x Quad-Pumped Signals. These signals include D[63:00]# and DBI[3:0]#. The signals are latched using dedicated strobes, STBP[3:0] and STBN[3:0], and then four-way demultiplexing is performed on these signals. The LAI inverts the appropriate signals when the DBI[3:0] signals are active.

2x Double-Pumped Signals. These signals include A[39:03]# and REQ[4:0]#. The LAI buffers and restores these signals. It then sends the signals to the logic analyzer along with ADSTB[0] to be multiplexed into the common clock domain. The logic analyzer uses the ADS to deterministically place these signals into the correct clock frame.

1x Common-Clock Signals. These signals include all of the remaining front side bus signals. The logic analyzer latches these signals using the rising edge of BCLK.

Signal Probing

The probe head uses passive series isolation to acquire data.

GTLREF Jumper Settings

The preprocessor unit uses reference voltages from the target system to derive a signal called GTLREF_AVG. This voltage is used as a reference to acquire most signals from the target system. The preprocessor unit can average up to five reference voltages and a manual offset voltage. See *Configure the Preprocessor Unit* beginning on page 3.

Accessories

Standard Accessory

The following standard accessory is shipped with the TMSST2 preprocessor unit:

Quantity	Accessory	Part number
1	MICRO SUPPORT; SW; PUB32G11,W/HARDWARE MANUAL;TMSST2	063-3835-XX
1	ACCESSORY KIT; LGA771 HEAT SINK;TMSDPH2	020-2650-XX
1	ACCESSORY KIT; LGA775 HEAT SINK;TMSDPH2	020-2708-XX

Optional Accessories

The following optional accessories are available for the TMSST2 preprocessor unit:

Option	Description	Part number or product name
-	LA PROBE; LOGIC ANALYZER PROBE FOR TLA7AXX,34 CHANNEL,HIGH DENSITY COMPRESSION,SINGLE ENDED/DIFFERENTIAL CLOCK,SINGLE ENDED DATA	P6860[1]
-	TMS PREPROCESSOR CABLE ASSEMBLY W/ LABELS	TMSCAB1[2]
	TMSDPH2 PROBE HEAD BOARD W/CABLES & PADDLE BD,SOCKET T/J 771/775 LGA	TMSDPH2
-	MICRO SUPPORT; SW; IA32G11,MICROPROCESSOR SUPPORT,RUL 2, W/PDF MANUAL TMS119 & TMSST2	063-3838-XX[3]
-	PROBE HEAD; SOCKET F 604 PIN. CERTIFICATE OF TRACEABLE CALIBRATION STANDARD WITH PRODUCT.	TMSSPH1
	MICRO SUPPORT; SW;PUB32G16, MICROPROCESSOR SUPPORT, W/PDF MANUAL TMSSPH1 PROBE HEAD;INCLUDES 071200100	063-3982-XX
-	MICRO SUPPORT; SW; IA32G16; MICROPROCESSOR SUPPORT, RUL *2, W/PDF MANUAL TMS125 & TMSST2	063-3968-XX[3]
-	SHIPPING KIT: CARTON AND FOAM	065-0701-XX
-	PLASTIC STORAGE CASE WITH FOAM INSERTS AND FLEX CABLE ASSEMBLY	016-1940-XX
A0	US POWER CORD. (STANDARD ACCESSORY)	161-0104-00
A1	UNIVERSAL EURO POWER CORD	161-0104-06
A2	UNITED KINGDOM POWER CORD	161-0104-07
A5	SWITZERLAND POWER CORD	161-0167-00

1 Requires six probes

2 Requires five cables

3 This support software is available only to customers with a valid, restricted, and secret nondisclosure agreement (RS- NDA) with Intel and Tektronix.

TMSCAB1 Labels

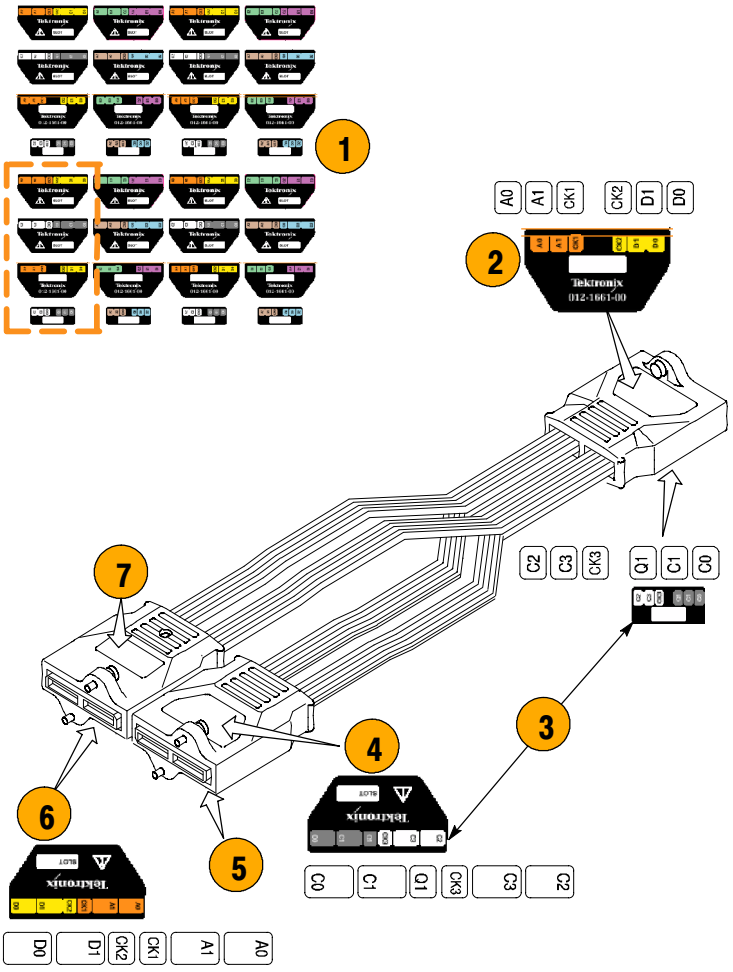
If you need to attach labels to the module end and the preprocessor end of theTMSCAB1 cables, use the following instructions.

***NOTE**. Always use flat-nosed tweezers to remove the labels from the sheet of labels. Never peel labels with your fingers. The labels are made of soft vinyl and can stretch and distort easily. To avoid stretching the label, always grasp it from the top right corner while removing it from the sheet of labels.*

The adhesive on the vinyl labels is extremely strong. Carefully align the label to the indented outline on the module end and preprocessor unit end. Once labels are placed on the TMSCAB1 cables, they are difficult to remove.

Follow these steps to attach the labels:

1. Determine which channel groups you plan to use and identify the matching labels.
2. Align and place the label in the label indent (preprocessor-unit end).
3. Match the color and the channel name.
4. Align and place the label in the label indent (module end)
5. No label on the underside of this connector.
6. Align and place the label in the label indent (module end).
7. No label on this side of the connector.



Probe Adapter Notes

Probe Adapter Notes

Review electrical, environmental, and mechanical specifications in the *Specifications* section starting on page 23 because they pertain to the target system, and to the following information.

Acquisition before Reset. If data is acquired before a processor Reset signal is observed by the preprocessor unit, the data acquired by the logic analyzer will be inaccurate.

Data Bus. The TMSST2 product supports only a quad-pumped data bus.

Address Bus. The TMSST2 product supports only a double-pumped address bus.

Disabling the Cache (disassembly). The cache bus is not observable; therefore, disassembly requires that the cache must be disabled. Disabling the cache makes all instruction prefetches visible on the bus so that they are acquired, displayed, and correctly disassembled.

Maintenance

Before cleaning this product, read the following information:

CAUTION. *To prevent static damage to the microprocessor and the probe head, handle components only in a static-free environment. Always wear a grounding wrist strap, heel strap, or similar device while handling themicroprocessor and probe head.*

The probe head does not require scheduled or periodic maintenance. However, to keep good electrical contact and efficient heat dissipation, keep the probe head free of dirt, dust, and contaminants. When not in use, store the probe head in the original case and cardboard carton.

External Cleaning Only

Clean dirt and dust with a soft bristle brush. For more extensive cleaning, use only a damp cloth moistened with deionized water; do not use any other chemical cleaning agents.

WARNING. *To prevent personal injury or damage to the probe head, do not allow any moisture inside the probe head. Refer servicing of external parts in the probe head to only Tektronix authorized personnel. External parts may be replaced by qualified service personnel.*

CAUTION. *To prevent damage to the sensitive probe head cables, handle them with care.*

Storage

Short-Term Storage

For short-term storage, use the existing cardboard carton and packaging, and follow these steps:

1. Power off the DUT and the preprocessor unit. It is not necessary to power off the logic analyzer.
2. Reverse heat sink instructions (for LGA775 or 771 socket) to remove the heat sink.
3. Reverse steps 1 through 15 on page 10 to remove the probe head, dressing the cables so they are not pinched or contacting any sharp objects. When you fold the preprocessor cables use a minimum radius of 0.25-in (0.64 cm) at the fold.
4. Using non-static generating tape, tape the socket cover onto the pin header on the bottom of the probe head.
5. Store the probe head in the black case it was shipped in.

Long-Term Storage

For long-term storage, use the existing cardboard carton and packaging, and follow these steps:

1. Complete steps 1 through 5 on page 20 in the *Short-Term Storage* procedure.
2. Disconnect the preprocessor unit from the logic analyzer by removing the probes and TMSCAB1 cables from the top of the preprocessor unit.
3. Place the preprocessor unit and probe head inside static-shielding bags.
4. Place foam on the bottom and inside of the cardboard carton.
5. Place the foam end caps on both sides of the preprocessor unit and place the preprocessor unit inside the cardboard carton.
6. Place cables carefully over the top of the preprocessor unit.
7. Place probe head and cables in the appropriate cutouts.
8. Place other accessories in the accessory tray.
9. Close and tape the cardboard carton.

Shipping the Probe Head

Contact the Service Center to obtain an RMA (return material authorization) number.

To commercially transport the preprocessor unit and probe head, package as follows:

1. Use the existing cardboard shipping carton and cushioning material. Follow the steps on page 21 to package the probe head and preprocessor unit.

   If the existing shipping carton is not available, use a double-walled, corrugated cardboard shipping carton that allows a 3-in (7.62 cm) minimum space on all sides of the product. Fill this space with nonstatic packing material.

2. If you are shipping a preprocessor unit or probe head to a Tektronix service center for warranty service, attach a tag to the product showing the following:
   - The RMA number
   - Owner's name and address
   - Name of a person who can be contacted
   - Probe head type and serial number
   - Description of the problem

Mark the address of the Tektronix Service Center and the return address on the shipping carton in two prominent locations.

Specifications

These specifications are for a probe adapter (preprocessor unit and probe head) that is connected between a compatible Tektronix logic analyzer and a target system. All specifications are typical. This section also outlines the electrical and mechanical requirements that the system-design engineer must observe during the planning and designing of their target system. This planning ensures compatibility with the probe adapter.

***NOTE**. These specifications can be used with the TMSSPH1 probe head with the exception of the dimensional drawing, or noted otherwise.*

Reference Voltage

Some target systems incorporate multiple reference voltages. These voltages are averaged by the preprocessor unit and used to receive all signals. Figure 2 shows an example of averaging two different reference voltages.

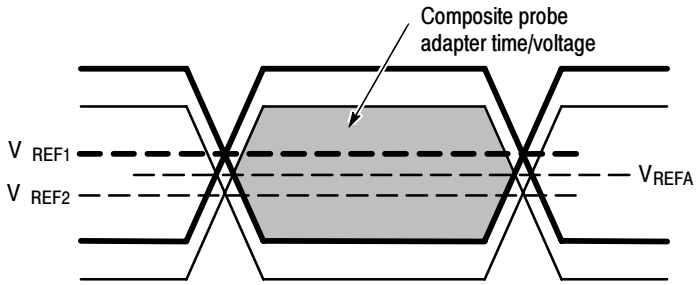


Figure 2: Multiple reference voltage averaging

***NOTE**. The overall time/voltage eye seen by the probe adapter is reduced when different reference voltages are present in the target system.*

When designing a multiple reference voltage system, the system designer must ensure that the composite eye seen by the preprocessor unit conforms to the electrical requirements described in this section. All electrical requirements listed in this section are relative to the averaged reference voltage.

The preprocessor unit provides a user-defined offset that can be added to the averaged reference voltage for flexibility. The offset function can also be used by itself, and adjusted to a desired fixed voltage. The averaged reference voltage tracks changes in the references, while the offset is a fixed voltage. To provide a significant amount of tracking while using an offset, the averaged reference is weighted 20:3 relative to the Offset voltage.

The TMSST2 preprocessor unit generates a separate termination and reference voltage.

With separate reference and termination voltages, it is possible to adjust the termination voltage to optimize target-system performance with the preprocessor unit installed and active. You can then adjust the reference voltage to optimize the preprocessor unit operation and achieve error-free acquisition. In most applications, the affect of the probe adapter loading is low enough to suffice for the simplest case of reference and termination voltages (both being set to the averaged reference only, no offset). Independent adjustments with or without offsets are available, if needed.

Table 8: GTLREF reference voltage requirements for the target system

Description	Min	Max
Input voltage range[1]	0.40 V	1.10 V
Input current (DC bias)[2]	-0.2 μA	0.2 μA
Offset voltage range, combined[3]	See Note[3]	See Note[3]
Offset voltage range, Offset only[4]	0.45 V	1.0 V
Slew Rate[5,7]	0	1.25 mV/μs
Edge Rate, 10-90%; ≤50mv step size[6,7]	40 μs	--
Edge Rate, 10-90%; 50mv < step ≤200mv[6,7]	50 μs	--

1 Specifications are relative to the pins on the probe head.

2 AC load modeled as unterminated 275 Ω, 8 ns transmission line.

3 Max Negative Offset = 0.13 x (V_{GTLREF_AVG} – 0.4);
Max Positive Offset = 0.13 x (1.0 – V_{GTLREF_AVG})

4 Fixed voltage, no tracking

5 Response is primarily bandwidth rather than slew rate limited.

6 Step response; transitions ≥20 μs for step sizes less than 50 μv, ≥30 μs for transitions up to 200 μv are stable within 100 μs. Faster transitions require up to 250 μs to stabilize.

7 Because of propagation delay and slew rate differences between V_{TERM} and V_{REF}, acquisition is not guaranteed to be error-free during reference voltage transitions that violate the Slew Rate or Edge Rate limits.

AC/DC Signaling

The TMSST2 preprocessor unit divides the front side bus signals into different acquisition groups depending on the characteristics of each signal. Each signal group is acquired using a different acquisition topology and has unique AC and DC requirements.

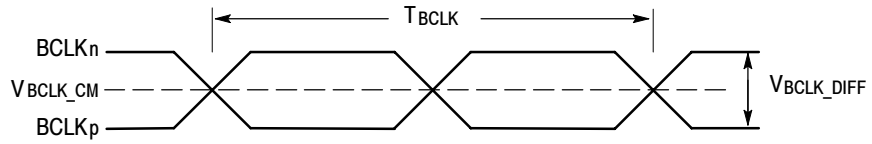


Figure 3: BCLK requirements

Table 9: BCLK requirements for the target system

Symbol[1,2,3]	Description	Min	Max
---	Common Clock Rate[1]	100 MHz	333 MHz[4]
T_{BCLK}	Clock period	3 ns[4]	10 ns
V_{BCLK_DIFF}	Differential input voltage	200 mV	900 mV
V_{BCLK_CM}	Differential common-mode input range	0.15 V	1.1 V

1 Specifications are relative to the pins on the probe head.

2 Uncertainty surrounding the active edge is accounted for in the requirements of the signals that are latched by the active edge.

3 Signal must be monotonic during transition.

4 TMSSPH1 common clock rate is 267 MHz, 3.75 ns.

Strobe Signals

There are two strobe signal acquisition groups. Each group is defined in the table below, followed by the AC and DC signaling requirements. Both strobe groups have the same requirements.

Table 10: Strobe signal group assignments

Group	Signals	Description
DSTB	DSTB[3:0]p, DSTB[3:0]n	Single-ended, active falling-edge, buffered and used for latching solely by the preprocessor unit
ADSTB	ADSTB[1:0]	Single-ended, active on both edges, buffered initially by the preprocessor unit then used for latching by the LA module

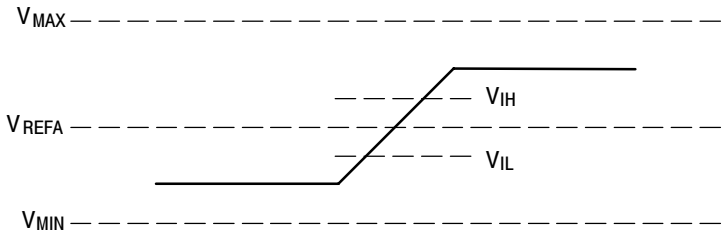


Figure 4: Strobe signal group requirements

Table 11: DSTB strobe signal requirements for the target system

Symbol[1,2,3,4]	Description	Requirement
V_{IH}	Input high voltage (min)	V_{REFA}+125 mV
V_{IL}	Input low voltage (max)	V_{REFA}-125 mV
V_{MAX}	Maximum input voltage	1.5 V
V_{MIN}	Minimum input voltage	-0.2 V

1 Specifications are relative to the pins on the probe head.

2 Uncertainty surrounding the active edge is accounted for in the requirements of the signals that are latched by the active edge.

3 Signal must be monotonic during transition.

4 V_{IH}, V_{IL} are dependant upon the receiver hysteresis setting. Larger hysteresis yields larger delay changes due to changes in required overdrive and thus larger Setup and Hold window size. Selected hysteresis is relatively large, thus yielding substantial noise immunity but requiring a substantial overdrive.

To improve immunity to nonmonotonic anomalies present on the target system strobe signals, the preprocessor and logic analyzer module employ both voltage and time domain hysteresis.

For both the DSTB and ADSTB signal groups, the voltage domain hysteresis is adjustable at the factory from 3.5 mV typical to over 100 mV at the probe tip. The amount of hysteresis applied cannot be changed. The amount of hysteresis is set to nominally 48 mV ($\pm$24 mV).

The time domain hysteresis is different for the DSTB and ADSTB groups. For the DSTB group, any nonmonotonic anomaly within 0.8 ns of an incident falling-edge is ignored. For the ADSTB group, any nonmonotonic anomaly within 1250 ps of the incident falling or rising edge is ignored.

Latched Signals

Table 12: TMSST2 latched signal group assignments

Group	Signals	Latching edge	Description
L1 (LGA771 and 775 sockets)	BNR, BPM[5:0], BPRI, BR[1:0], DBSY, DEFER, FERR, IERR, LINT[1:0], LOCK, NMI, MCERR, PROCHOT, RSP, THERMTRIP, TRDY	BCLK	275 Ω load, terminated to V_{TERM}; latched by LA module
L1 (PGA604 socket)	BNR, BPM[5:0], BPM_2[3:0], BPRI, BR[1:0], DBSY, DEFER, FERR, IERR, LINT[1:0], LOCK, NMI, MCERR, PECI, RSP, SKTOCC, TRDY	BCLK	275 Ω load, terminated to V_{TERM}; latched by LA module
	THERMTRIP		Unterminated 75 Ω, 8 ns transmission line w/ 200 Ω series resistor at Interposer; latched by LA module.
L2[1] (LGA771 and 775 sockets)	A20M, IGNNE, INIT, SMI, STPCLK, TCK, TDI, TDO, TMS, TRST	BCLK	275 Ω load, terminated to $0.75xV_{GTLREF\_AVG}$, latched by LA module
	PWRGOOD		Unterminated: 75 Ω, 8 ns transmission line w/ 200 Ω series resistor at Interposer
L2[1] (PGA604 socket)	A20M, IGNNE, INIT, SMI, STPCLK	BCLK	275 Ω load, terminated to $0.75xV_{GTLREF\_AVG}$, latched by LA module
	TRST, TMS, TDO_M, TDO, TDI_M, TDI, TCK		Unterminated: 75 Ω, 8 ns transmission line w/ 200 Ω series resistor at Interposer
L3	ADS, BINIT, DRDY, HIT, HITM, RESET, RS[2:0]	BCLK	275 Ω load, terminated to V_{TERM}; latched by preprocessor unit for real-time processing, also latched by LA module.
L4	A[39:3], REQ[4:0]	ADSTB	275 Ω load, terminated to V_{TERM}; latched by LA module.
L5	D[63:0], DBI[3:0]	DSTB	275 Ω load, terminated to V_{TERM}; latched by preprocessor unit for real-time processing.

1 Commonly referred to as CMOS

Figure 5 and Table 13 show the requirements for each of the latched acquisition groups. Each group defines a four-point time/voltage eye that is measured relative to the respective latching edge and V_{REFA}. LX represents the group name in Figure 5. For example, if you are using Group L1, LX equals L1.

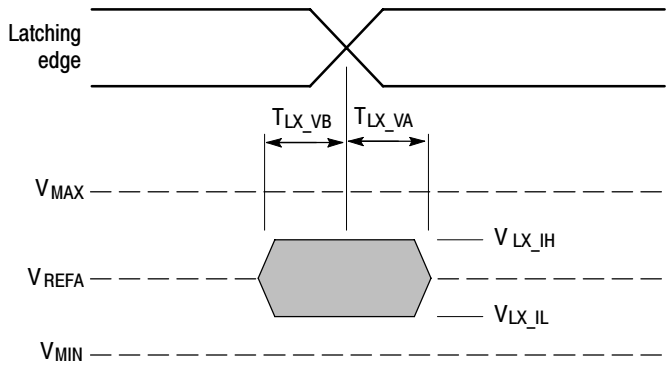


Figure 5: Latched signal group requirements

Table 13: Latched signal requirements for the target system

Symbol	Description	Typical
T_{L1_VB}[1,2,3]	L1 valid time before edge	800 ps
T_{L1_VA}[1,2,3]	L1 valid time after edge	100 ps
V_{L1_IH}[1,2,3]	L1 input high voltage	V_{REFA}+150 mV
V_{L1_IL}[1,2,3]	L1 input low voltage	V_{REFA}-150 mV
T_{L2_VB}[1,2,3]	L2 valid time before edge	850 ps
T_{L2_VA}[1,2,3]	L2 valid time after edge	150 ps
V_{L2_IH}[1,2,3]	L2 input high voltage	0.75*V_{GTLREF_AVG} +150 mV
V_{L2_IL}[1,2,3]	L2 input low voltage	0.75*V_{GTLREF_AVG} -150 mV
T_{L3_VB}[1,2,3]	L3 valid time before edge	750 ps
T_{L3_VA}[1,2,3]	L3 valid time after edge	50 ps
V_{L3_IH}[1,2,3]	L3 input high voltage	V_{REFA}+150 mV
V_{L3_IL}[1,2,3]	L3 input low voltage	V_{REFA}-150 mV
T_{L4_VB}[1,2,3]	L4 valid time before edge	400 ps
T_{L4_VA}[1,2,3]	L4 valid time after edge	400 ps
V_{L4_IH}[1,2,3]	L4 input high voltage	V_{REFA}+125 mV
V_{L4_IL}[1,2,3]	L4 input low voltage	V_{REFA}-125 mV
T_{L5_VB}[1,2,3]	L5 valid time before edge	250 ps
T_{L5_VA}[1,2,3]	L5 valid time after edge	250 ps
V_{L5_IH}[1,2,3]	L5 input high voltage	V_{REFA}+75 mV
V_{L5_IL}[1,2,3]	L5 input low voltage	V_{REFA}-75 mV

Table 13: Latched signal requirements for the target system (Cont.)

Symbol	Description	Typical
V_{MAX}[1,4]	Maximum input voltage (all signals excluding unterminated L2)	+1.5 V
V_{MIN}[1,4]	Minimum input voltage (all signals excluding unterminated L2)	-0.2 V
V_{MAX}[1,4]	Maximum input voltage (unterminated L2)	+1.1 V
V_{MIN}[1,4]	Minimum input voltage (unterminated L2)	+0.1 V

1 Specifications are relative to the pins on the probe head.

2 Assumes nominal signal receiver hysteresis of 5 mV (no added hysteresis)

3 Timing characterized with both a pattern generator and selected target platforms; correlation to operation in the target environment is approximate due to edge rate and signal quality differences for both the measured signal and its strobe (clock) for different platforms.

4 Max and Min numbers rely on termination and thus GTLREF specified voltage limits.

Table 14 lists the electrical requirements for the power supply that provides power to the probe adapter. Table 15 lists the environmental specifications.

Table 14: Electrical specifications for AC input to the preprocessor unit

Characteristics	Description
Input Voltage rating	100 - 240 VAC ± 10%
Input Frequency Rating	50 - 60 Hz
Input Current Rating	6.0 A maximum

Table 15: Environmental specifications

Characteristic	Description
Temperature[2]	Operating: 5 °C to +50 °C (+41 °F to +122 °F)[1] Nonoperating: -55 °C to +75 °C (-67 °F to +167 °F)
Electrostatic immunity	The probe adapter is static sensitive
Weight	
Preprocessor unit plus power cord	11.4 Kg (25 lbs)
Shipping Weight	
Preprocessor unit plus cables, power cord, and packaging	24 Kg (53 lbs)

1 Not to exceed microprocessor thermal considerations. Customer supplied cooling might be required across the CPU.

2 Refer to the instruction manual for the TMSSPH1 probe head for temperature specifications.

Certifications and Compliances

EC Declaration of Conformity - EMC

Meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility when this product is used with the product(s) stated in the specifications table. Refer to the EMC specification published for the stated products. May not meet the intent of the Directive if used with other products.

EC Declaration of Conformity - Low Voltage

Compliance was demonstrated to the following specification as listed in the Official Journal of the European Communities:

Low Voltage Directive 73/23/EEC, amended by 93/68/EEC.

- EN 61010-1:2001. Safety requirements for electrical equipment for measurement control and laboratory use.

U.S. Nationally Recognized Testing Laboratory Listing

- UL 61010B-1:2003. Standard for electrical measuring and test equipment.

Canadian Certification

- CAN/CSA C22.2 No. 1010.1:1997. Particular requirements for electrical equipment for measurement, control, and laboratory use. Part 1.

Equipment Type

Test and measuring equipment

Safety Class

Class 1 - grounded product

Pollution Degree Descriptions

A measure of the contaminates that could occur in the environment around and within a product. Typically the internal environment inside a product is considered to be the same as the external. Products should be used only in the environment for which they are rated.

- Pollution Degree 1. No pollution or only dry, nonconductive pollution occurs. Products in this category are generally encapsulated, hermetically sealed, or located in clean rooms.
- Pollution Degree 2. Normally only dry, nonconductive pollution occurs. Occasionally a temporary conductivity that is caused by condensation must be expected. This location is a typical office/home environment. Temporary condensation occurs only when the product is out of service.
- Pollution Degree 3. Conductive pollution, or dry, nonconductive pollution that becomes conductive due to condensation. These are sheltered locations where neither temperature nor humidity is controlled. The area is protected from direct sunshine, rain, or direct wind.
- Pollution Degree 4. Pollution that generates persistent conductivity through conductive dust, rain, or snow. Typical outdoor locations.

Pollution Degree

Pollution Degree 2 (as defined in IEC 61010-1). Note: Rated for indoor use only.

Installation (Overvoltage) Category Descriptions

Terminals on this product may have different installation (overvoltage) category designations. The installation categories are:

- Measurement Category IV. For measurements performed at the source of low-voltage installation.
- Measurement Category III. For measurements performed in the building installation.
- Measurement Category II. For measurements performed on circuits directly connected to the low-voltage installation.
- Measurement Category I. For measurements performed on circuits not directly connected to MAINS.

Overvoltage Category

Overvoltage Category II (as defined in IEC 61010-1)

Loading Diagrams

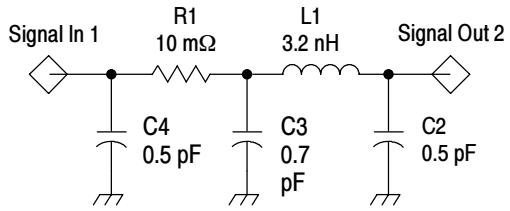


Figure 6: Mated Samtec load model

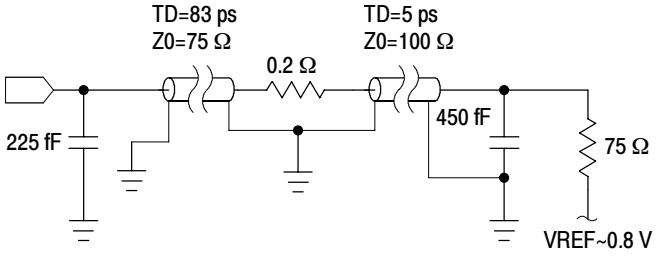


Figure 7: Receiver load model

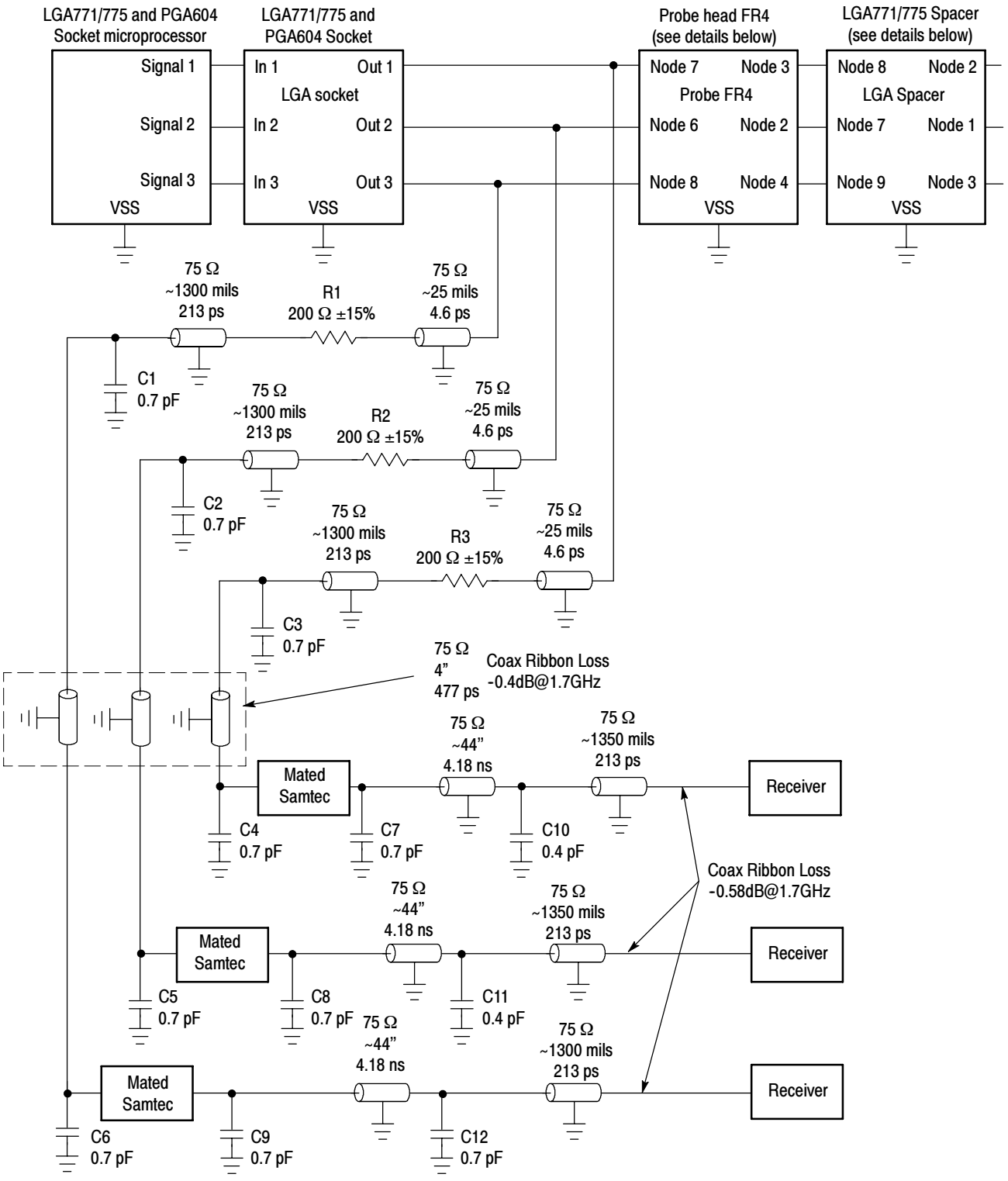


Figure 8: Electrical load model for typical signals

Dimensions

Figure 9 shows the dimensions of the TMSDPH2 probe head.

***NOTE**. For the TMSSPH1 probe head dimensions, refer to the product documentation.*

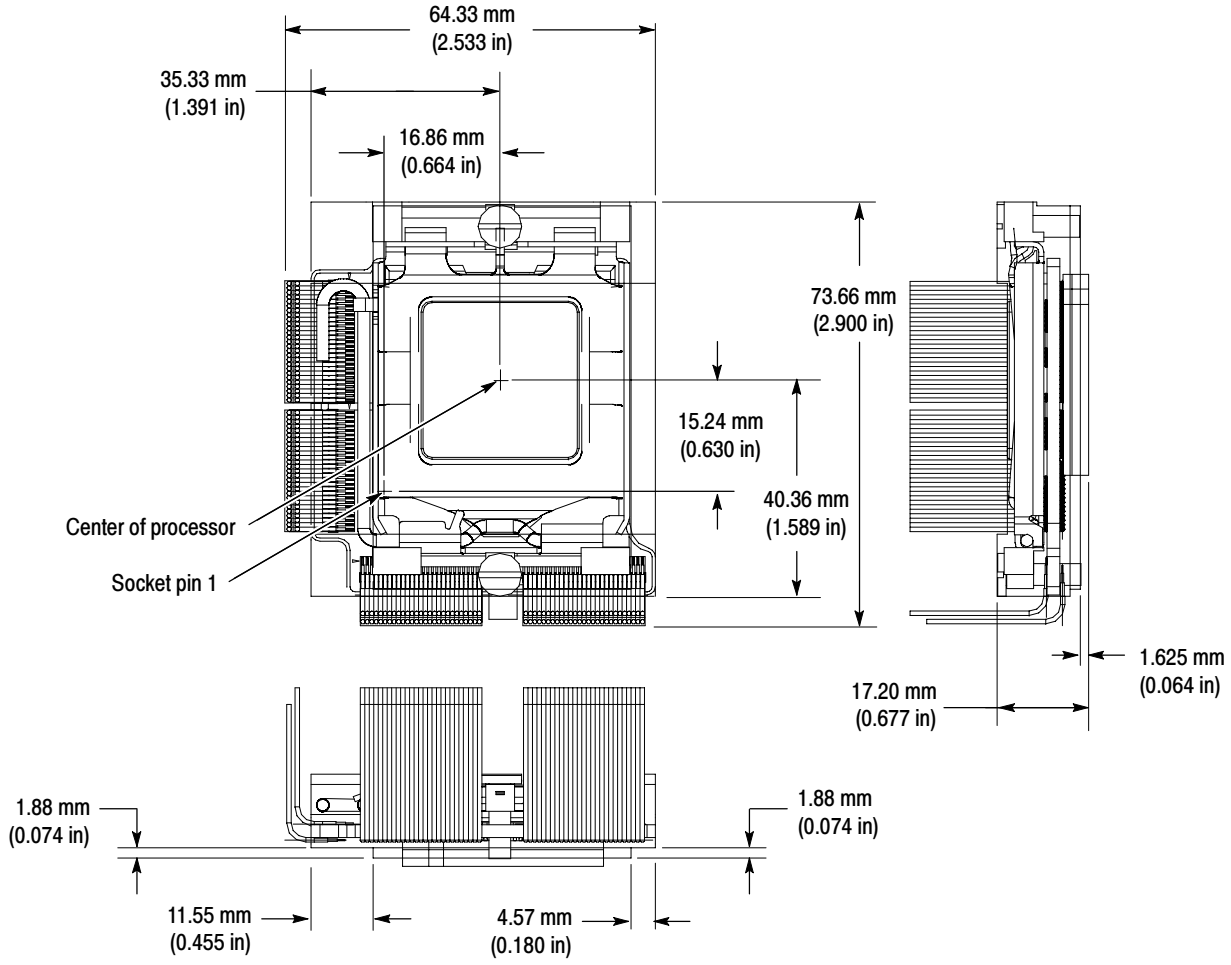


Figure 9: Dimensions of the probe head

Figure 10 shows the dimensions of the preprocessor unit.

CAUTION. *To prevent damage to the circuitry in the preprocessor unit, you must observe the required clearances in Table 7 on page 7 (clearances are not shown in Figure 10).*

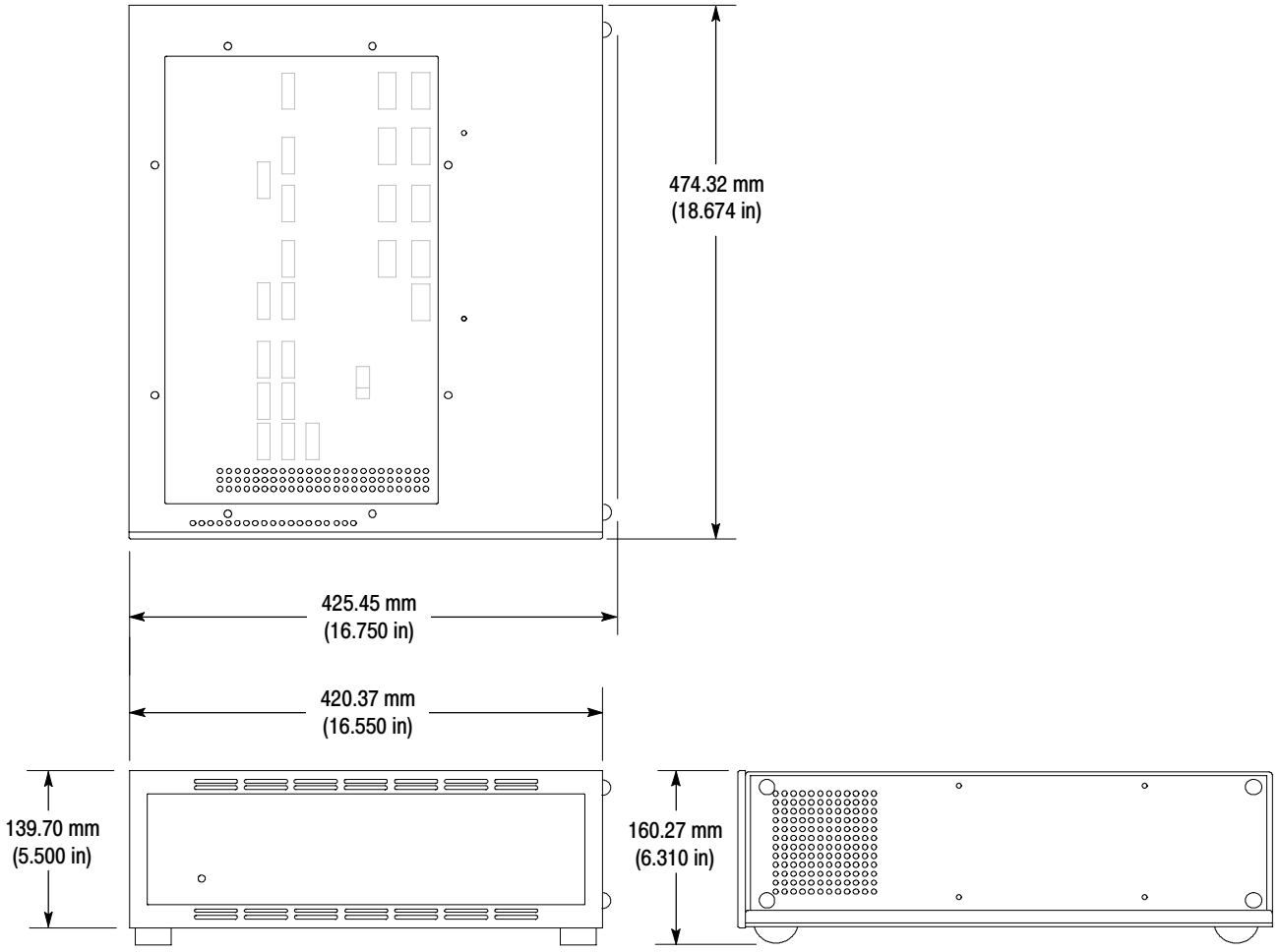


Figure 10: Dimensions of the preprocessor unit

Design Review Checklists

Table 16: General checklist

Yes	No	NA	Item
			Have you contacted Tektronix for any updates to the design information in this *Reference* section?

Table 17: Electrical checklist

Yes	No	NA	Item
			Have you performed electrical simulations with the probe adapter load models[1]?
			Will the target system operate with the additional probe adapter load[1]?
			Are the electrical requirements described in this *Reference* section satisfied?
			If the target system uses multiple reference voltages, does the composite time and voltage eye meet the electrical requirements described in this *Reference* section? See Figure 2 on page 23.

1 See page 31 in the *Specification* section.

Table 18: Mechanical checklist

Yes	No	NA	Item
			Have you performed mechanical fit checks using the KOV ProE model[1]?

1 The detailed mechanical keep-out-volume (KOV) for the probe head is described using the ProE 3D modeling package. System designers should import the probe head KOV model into their modeling environment to ensure that the probe head can be placed in the platform without any interference. Contact your Tektronix sales representative to obtain the latest ProE probe head KOV model.

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